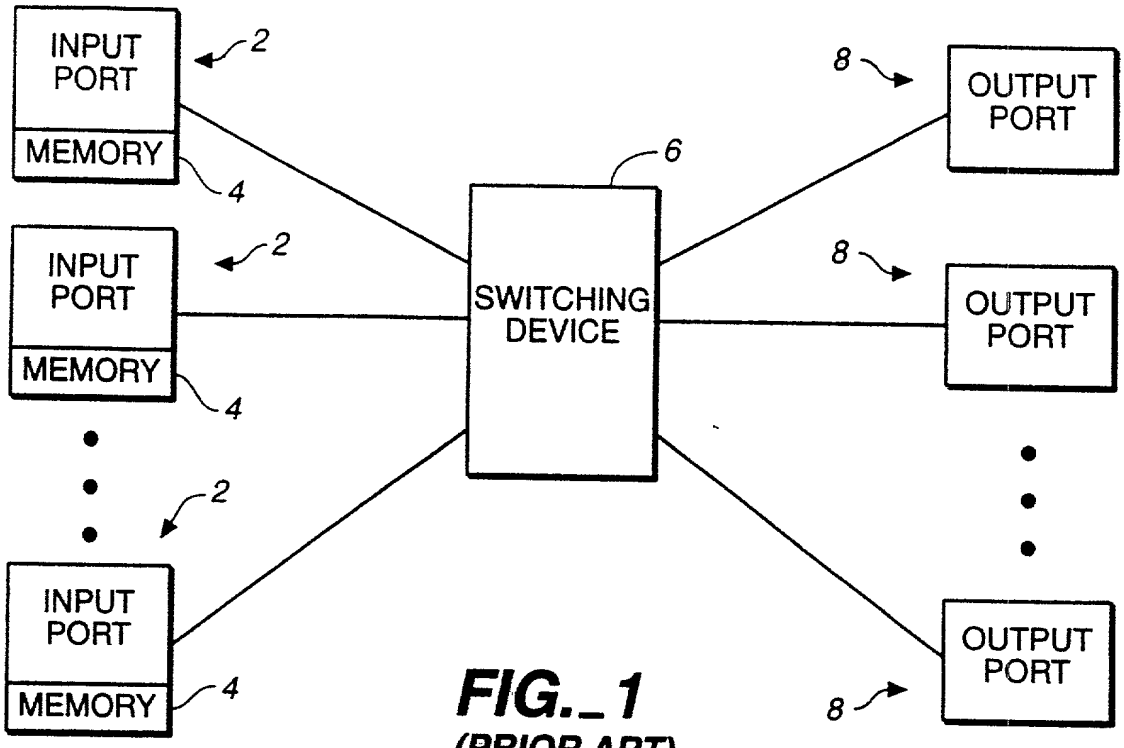

FIG._1
(PRIOR ART)

4,933,938 - 06/12/1990

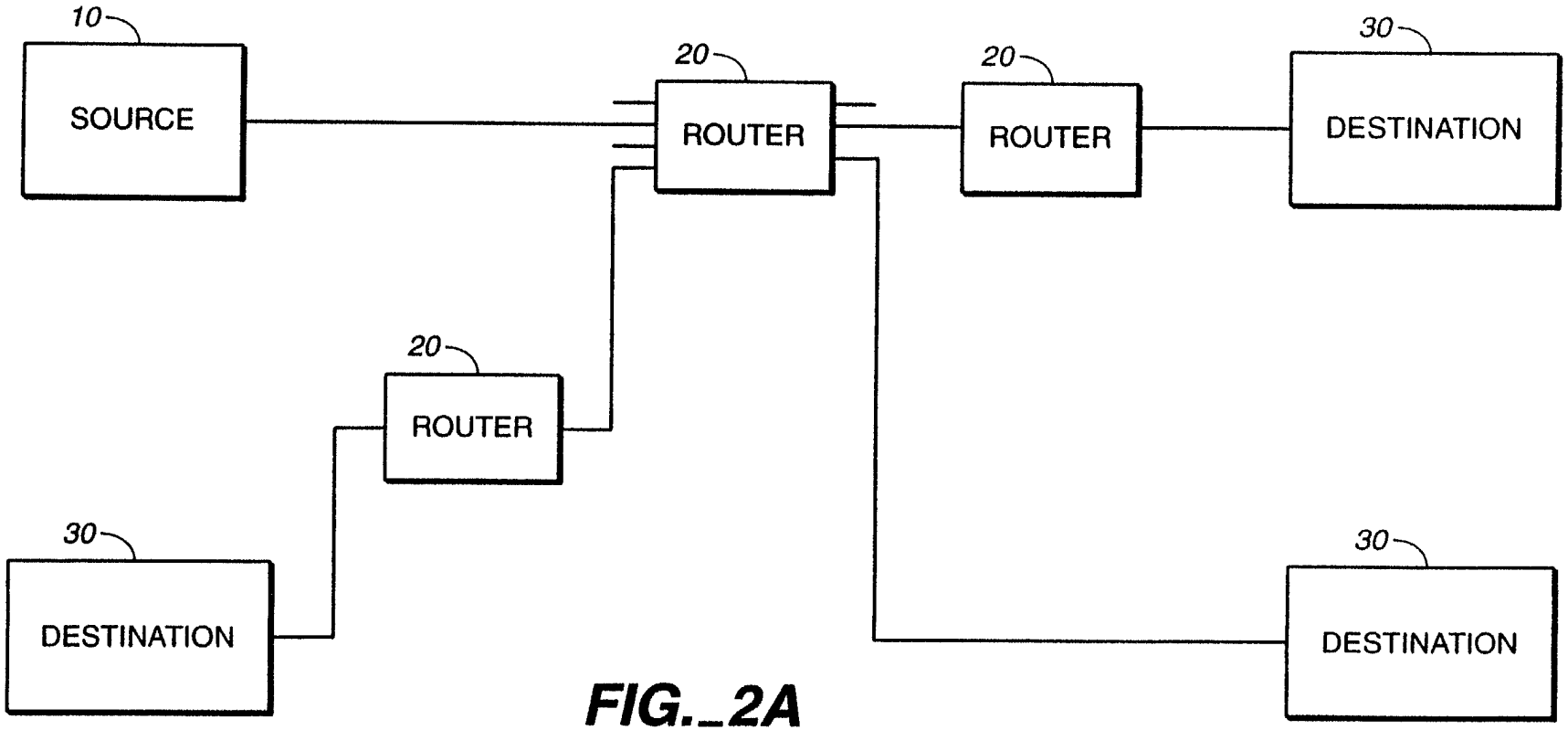
10
SOURCE
20
ROUTER
20
ROUTER
30
DESTINATION
20
ROUTER
30
DESTINATION
30
DESTINATION

FIG._2A

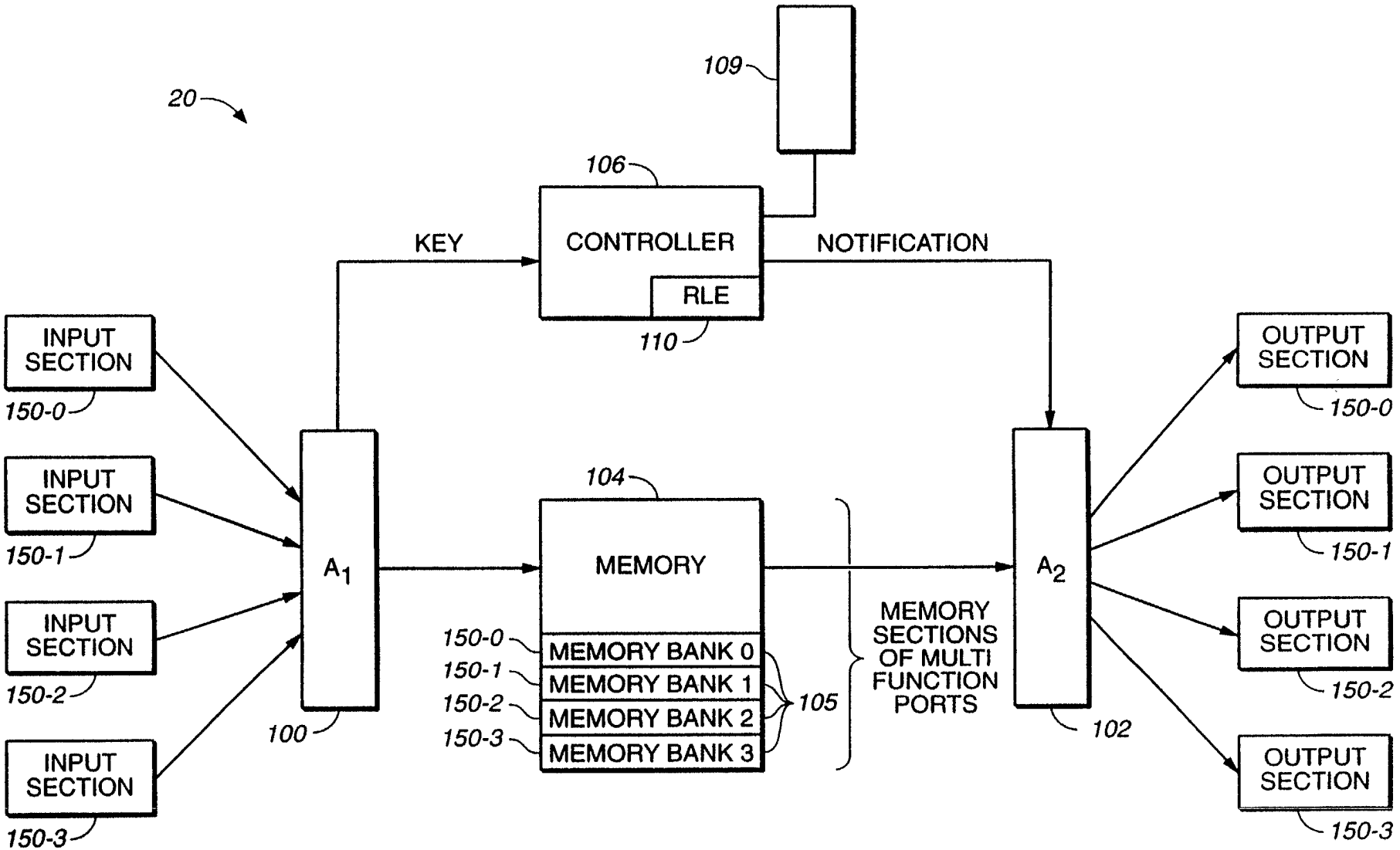
20
109
106
CONTROLLER
RLE
110
KEY
NOTIFICATION
INPUT SECTION
150-0
INPUT SECTION
150-1
INPUT SECTION
150-2
INPUT SECTION
150-3
A1
100
104
MEMORY
150-0
150-1
150-2
150-3
MEMORY BANK 0
MEMORY BANK 1
MEMORY BANK 2
MEMORY BANK 3
105
MEMORY SECTIONS OF MULTI FUNCTION PORTS
A2
102
OUTPUT SECTION
150-0
OUTPUT SECTION
150-1
OUTPUT SECTION
150-2
OUTPUT SECTION
150-3

FIG._2B

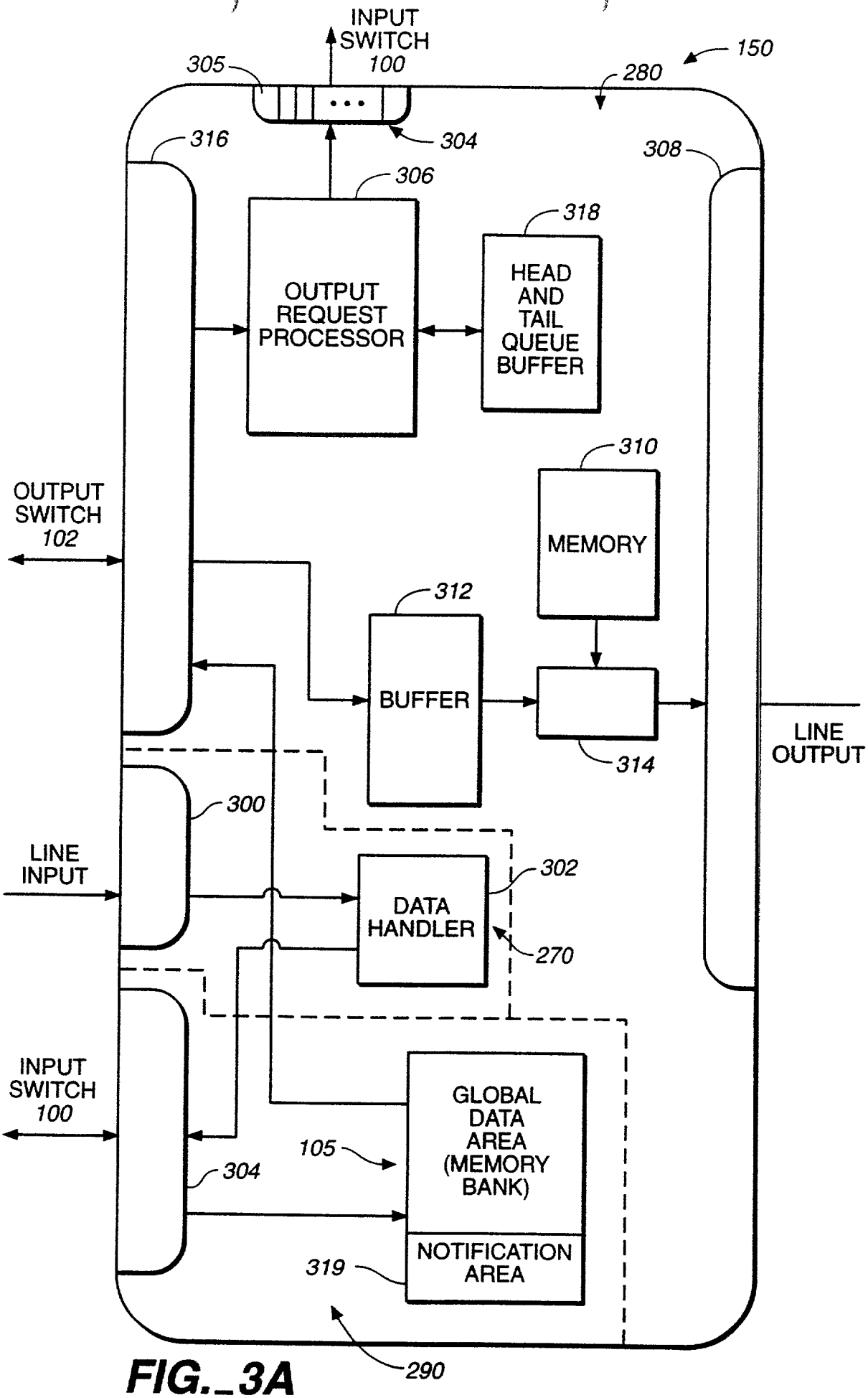
INPUT SWITCH 100
150
305
280
316
304
308
306
318
OUTPUT REQUEST PROCESSOR
HEAD AND TAIL QUEUE BUFFER
310
OUTPUT SWITCH 102
MEMORY
312
BUFFER
314
LINE OUTPUT
300
LINE INPUT
302
DATA HANDLER
270
INPUT SWITCH 100
GLOBAL DATA AREA (MEMORY BANK)
105
304
NOTIFICATION AREA
319
290

FIG._3A

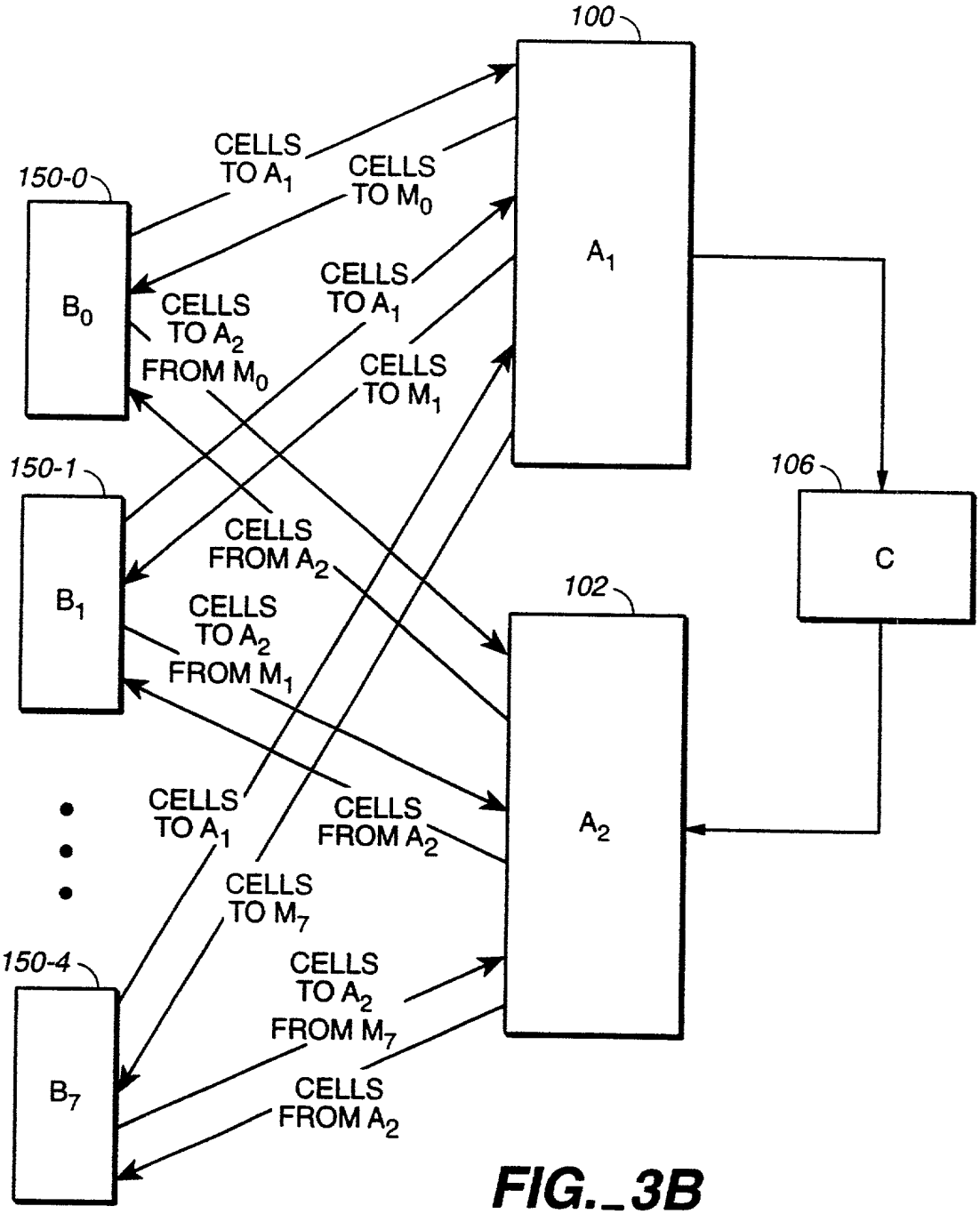
100
A1
150-0
B0
CELLS TO A1
CELLS TO M0
CELLS TO A2 FROM M0
CELLS TO A1
CELLS TO M1
150-1
B1
CELLS FROM A2
CELLS TO A2 FROM M1
106
C
102
A2
CELLS TO A1
CELLS FROM A2
CELLS TO M7
150-4
B7
CELLS TO A2 FROM M7
CELLS FROM A2

FIG._3B

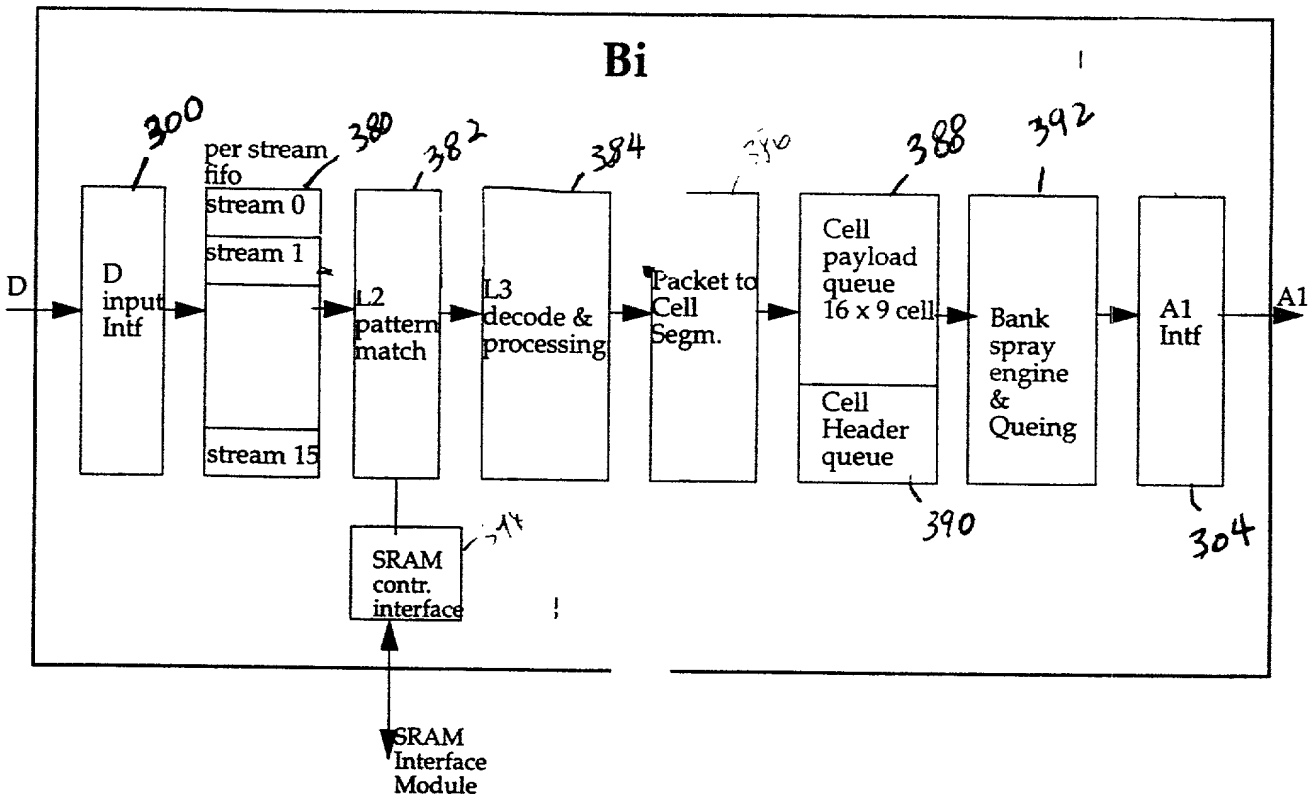
Bi
300
per stream fifo
380
382
384
386
388
392
D
D input Intf
stream 0
stream 1
stream 15
L2 pattern match
L3 decode & processing
Packet to Cell Segm.
Cell payload queue 16 x 9 cell
Cell Header queue
Bank spray engine & Queing
A1 Intf
A1
390
304
SRAM contr. interface
SRAM Interface Module

FIG 3C

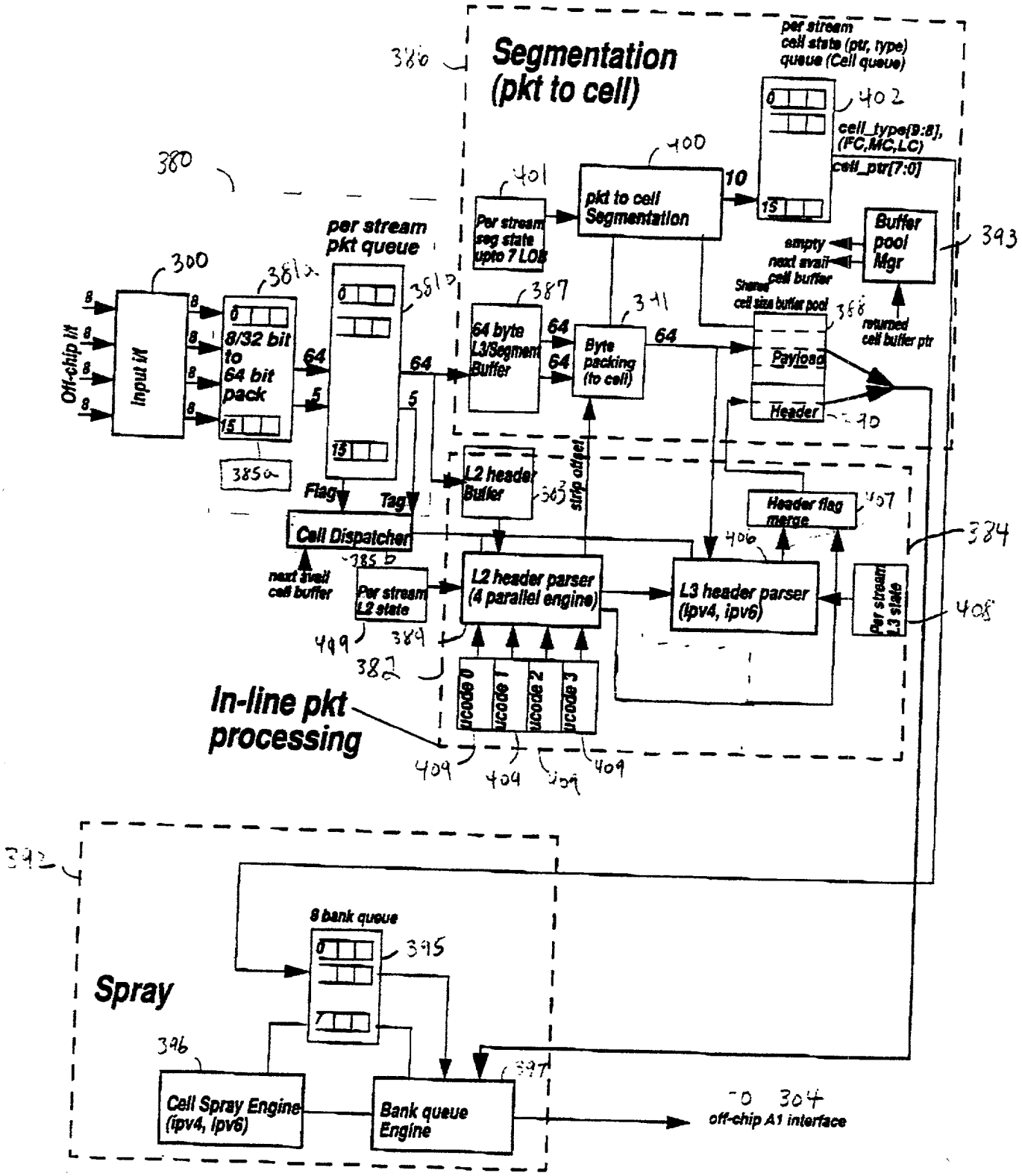
Segmentation (pkt to cell)
386
per stream cell state (ptr, type) queue (Cell queue)
402
cell_type[3:8], (FC,MC,LC)
cell_ptr[7:0]
400
pkt to cell Segmentation
401
Per stream seg state upto 7 LOs
10
15
Buffer pool Mgr
393
empty
next avail cell buffer
Shared cell size buffer pool
388
returned cell buffer ptr
380
per stream pkt queue
300
Off-chip I/f
Input I/f
8/32 bit to 64 bit pack
381a
381b
387
64 byte L3/Segment Buffer
341
Byte packing (to cell)
Payload
Header
390
385a
L2 header Buffer
363
strip offset
Flag
Tag
Cell Dispatcher
385b
next avail cell buffer
Per stream L2 state
389
L2 header parser (4 parallel engine)
L3 header parser (ipv4, ipv6)
Header flag merge
407
406
384
Per stream L3 state
408
382
ucode 0
ucode 1
ucode 2
ucode 3
In-line pkt processing
409
392
Spray
8 bank queue
395
396
Cell Spray Engine (ipv4, ipv6)
Bank queue Engine
397
TO 304
off-chip A1 interface

FIG 3d

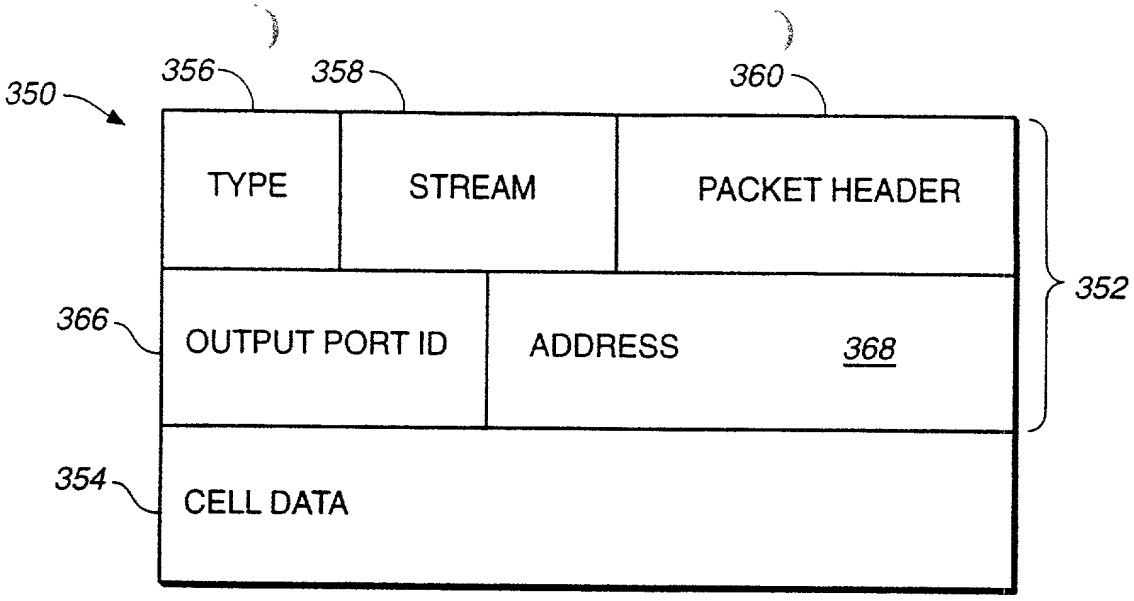
350
356
358
360
TYPE
STREAM
PACKET HEADER
352
366
OUTPUT PORT ID
ADDRESS
368
354
CELL DATA

FIG._3

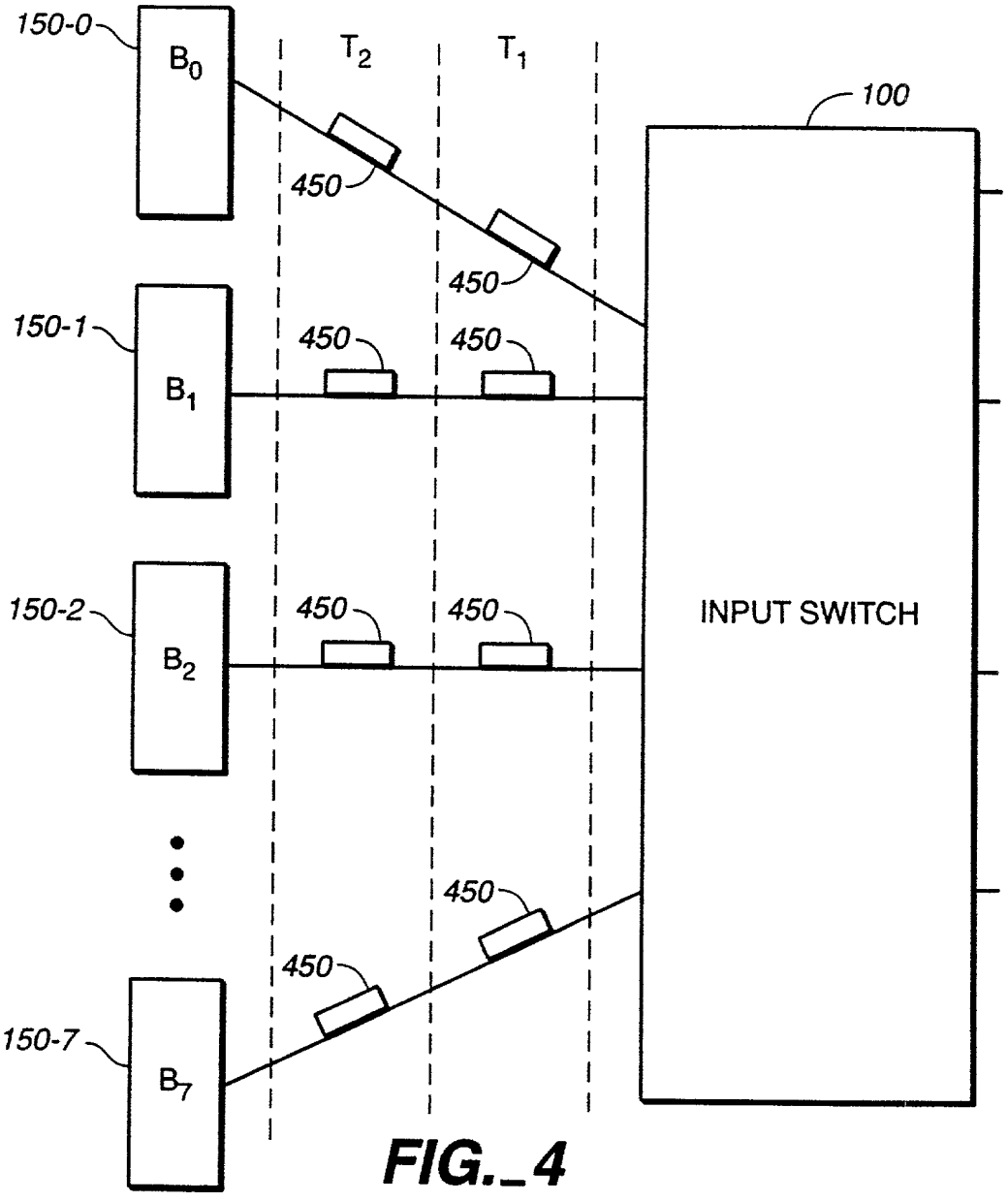
150-0
B0
T2
T1
100
450
450
150-1
B1
450
450
150-2
B2
450
450
INPUT SWITCH
450
450
150-7
B7

FIG._4

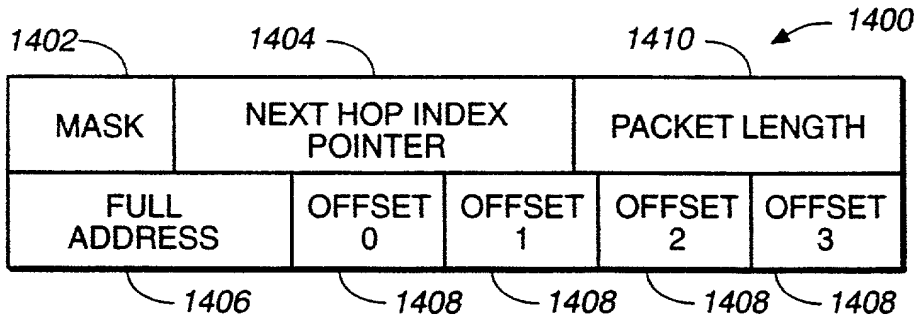
1400
1402
1404
1410
MASK
NEXT HOP INDEX POINTER
PACKET LENGTH
FULL ADDRESS
OFFSET 0
OFFSET 1
OFFSET 2
OFFSET 3
1406
1408
1408
1408
1408

FIG._ 5

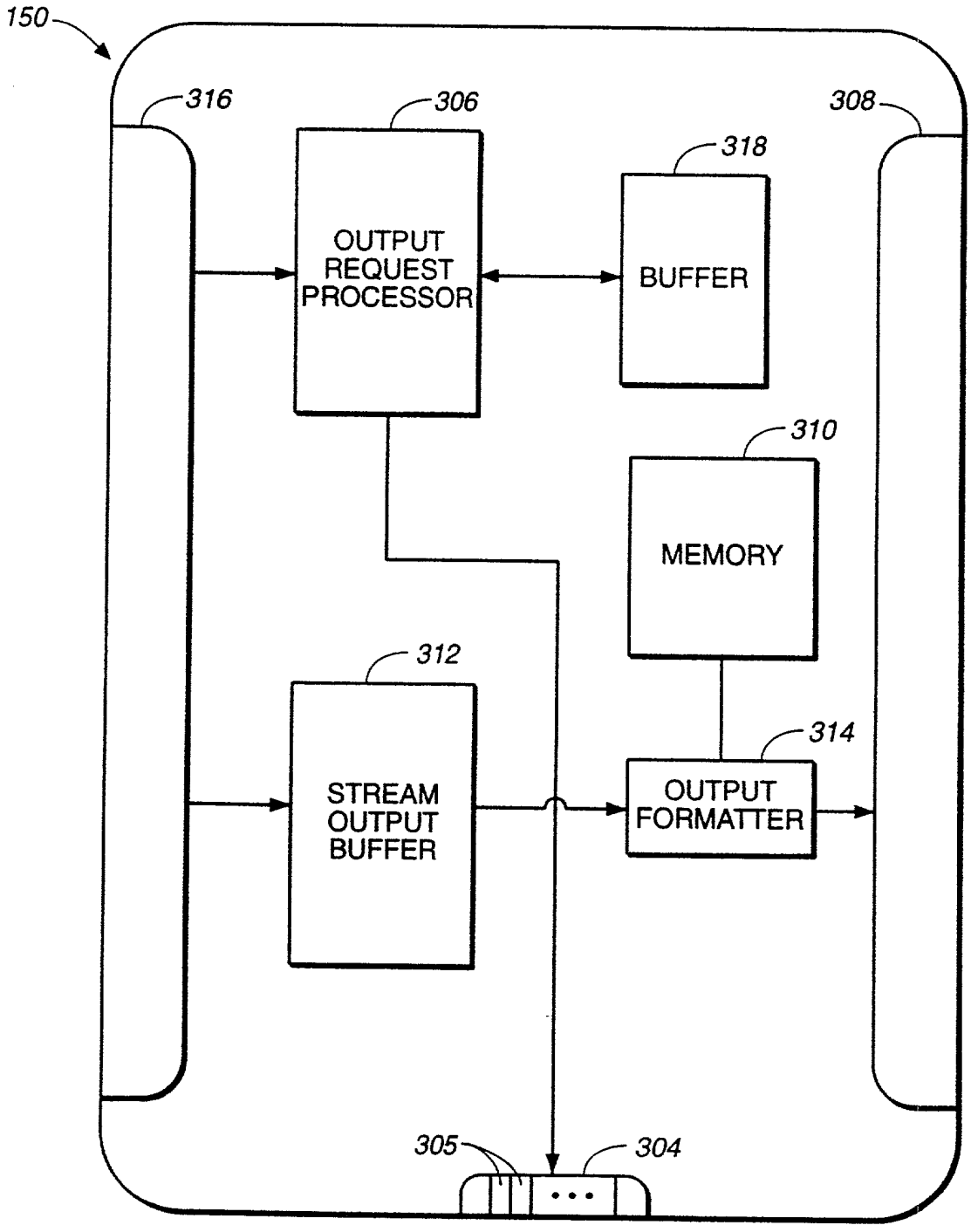
150
316
306
308
318
OUTPUT REQUEST PROCESSOR
BUFFER
310
MEMORY
312
STREAM OUTPUT BUFFER
314
OUTPUT FORMATTER
305
304

FIG._ 6

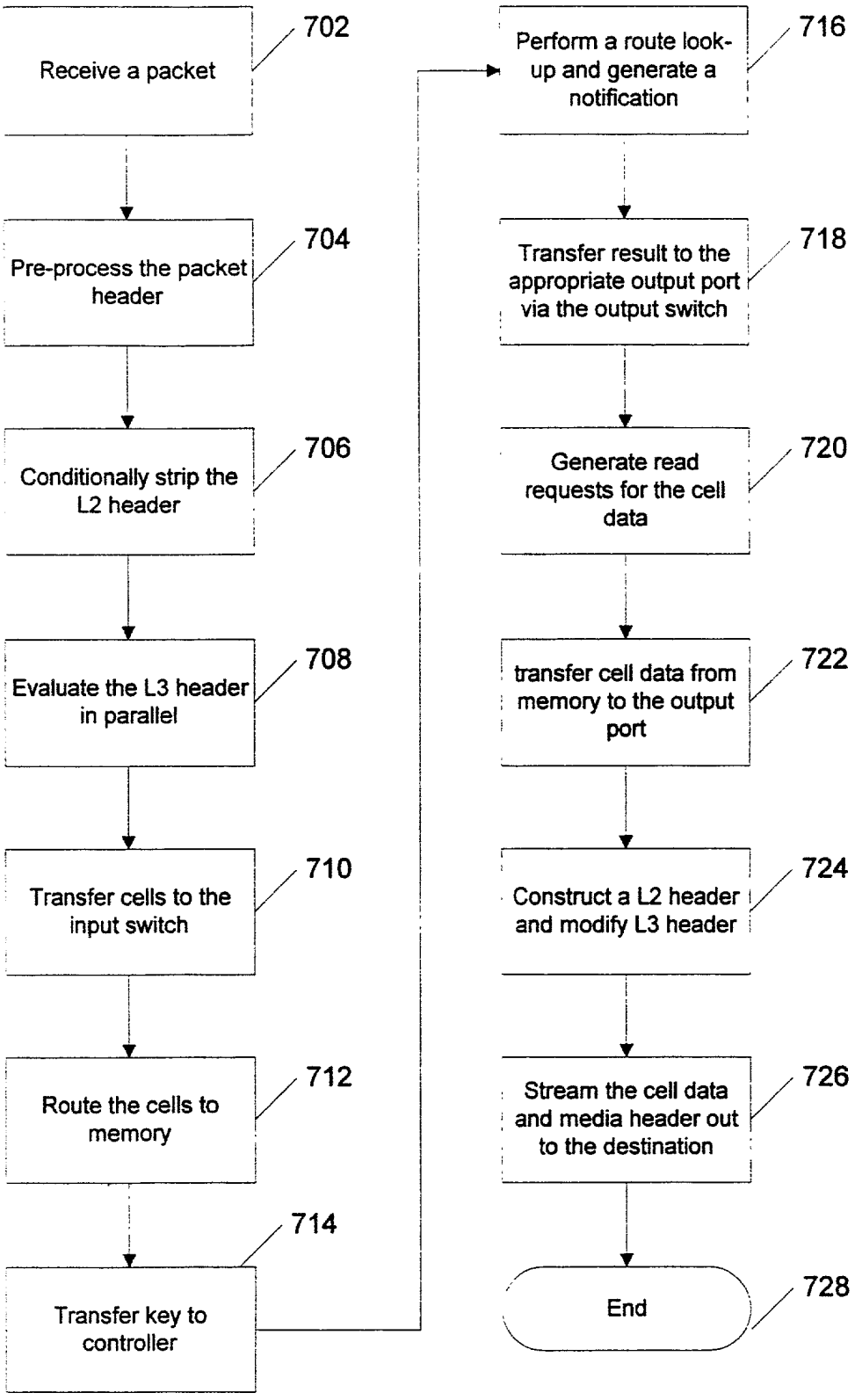
Receive a packet
702
Pre-process the packet header
704
Conditionally strip the L2 header
706
Evaluate the L3 header in parallel
708
Transfer cells to the input switch
710
Route the cells to memory
712
Transfer key to controller
714
Perform a route look-up and generate a notification
716
Transfer result to the appropriate output port via the output switch
718
Generate read requests for the cell data
720
transfer cell data from memory to the output port
722
Construct a L2 header and modify L3 header
724
Stream the cell data and media header out to the destination
726
End
728

Figure 7